ARC SUPPRESSION TECHNOLOGIES
7900 INTERNATIONAL DR STE 300, BLOOMINGTON, MN 55425
www.ArcSuppressionTechnologies.com

MYTHS & FACTS OF ARC-FLASH

Myths That Prevented Electronic Arc-Flash Suppression

By Reinhold Henke and Robert P. Thorbus

Commonly Heard Phrases and Common Statements of Belief

The electronic industry is rife with myths about arcs in general and arc-flash in specific. Consider the following myths that are commonly accepted and often repeated … in spite of being incorrect:

Myth: "An arc-flash is a short circuit!"

Fact: No, an arc-flash is actually a resistive load and is NOT a short circuit. The arc-flash plasma is a non-linear resistive load with a negative resistance causing a positive feedback effect with catastrophic results. The more current, the less resistance; the less resistance, the more current.

Myth: "Arc-flash energy can be easily calculated!"

Fact: No, arc-flash energy is NOT easily calculated[1] … however, a simplified calculation shows that about 90% of the energy is absorbed within the transformer, while about 10% is released via the arc-flash (tables I and 2; figures 1 and 2).

Myth: "The arc-flash is 'just like' a big contact arc !"

Fact: No, an arc-flash is NOT like a contact arc. A controlled contact arc's plasma burns is in series with a load, whereas, an uncontrolled arc-flash's plasma burns between the power conductors.

Myth: "Inductance in the loop is required for an arc!"

Fact: No, inductance in the loop is NOT required either to initiate an arc or to ignite an arc plasma. This myth may have gained credence, however, to inductance-in-the-loop being required to maintain, support, and extend the arc plasma burn duration once started.

Myth: "An arc is an Arc!"

Fact: No, all arcs are NOT the same. Every arc is a series of rather complex events, that differ by a variety of factors, including how they are initiated and how their plasma is ignited.[2,3]

Determining the Facts

The arc-flash myths & facts become apparent when one draws simplified, single phase, equivalent, schematic diagrams with a few elements forming one circuit loop, including: an ideal voltage source, in series with the internal voltage source resistor, in series with an NTC resistance as the load, representing the igniting and burning arc-flash plasma (figs. 1, 2). Such schematic diagrams enable designers to conduct appropriate engineering calculations to dispel myths.

An example comparison of a **bolted short circuit** (**BSC**) and an **arc-flash** (**AF**) is shown in tables I and II. The fact that calculated **AF** plasma energy is roughly 10% of total **BSC** energy shows that most of the energy is absorbed by the transformer. This energy difference also underscores that "arc-flash calculations" which measure total **BSC** energy do not accurately reflect actual **AF plasma energy**.

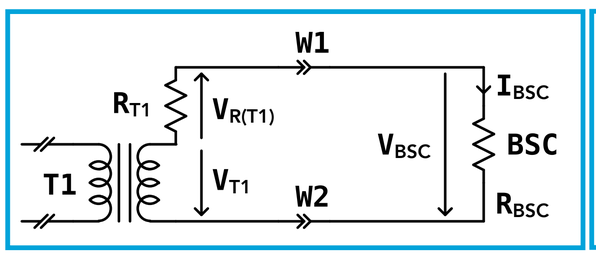

*Fig. 1: Simplified, equivalent schematic diagram for a Bolted Short Circuit (**BSC**); see table I*

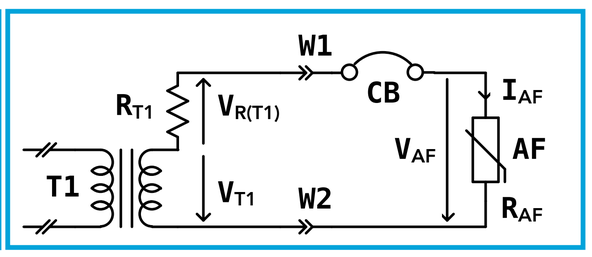

*Fig. 2: Simplified, equivalent schematic diagram for an Arc-Flash (**AF**); see table II*

Note: Infrastructure resistance and thermal effects are not included in these example calculations

T1 Secondary Open Circuit Voltage (nominal)	V_{T1}	480 V
T1 Bolted Short Circuit Current	$I_{T1(BSC)}$	20,000 A
Bolted Short Circuit Duration (comparison only)	T_{BSC}	0.167 s
Bolted Short Circuit Resistance (near zero)	R_{BSC}	0.000 Ω
T1 Internal Resistance	R_{T1}	0.0240 Ω
T1 Internal Power Dissipation During BSC	$P_{R(T1)}$	9,600,000 W
T1 Internal Energy Release During BSC	$W_{R(T1)}$	1,603,200 J

***Table I:** Bolted Short Circuit (**BSC**) parameters, symbols, & definitions; example of calculated or measured values; see figure 1*

T1 Secondary Open Circuit Voltage (nominal)	V_{T1}	480 V
T1 Bolted Short Circuit Current	$I_{T1(BSC)}$	20,000 A
Arc-Flash Duration	T_{AF}	0.167 s
Arc-Flash Voltage	V_{AF}	50 V
T1 Internal Resistance	R_{T1}	0.0240 Ω
T1 Internal Power Dissipation During AF	$P_{R(T1)}$	8,704,167 W
T1 Internal Energy Release During AF	$W_{R(T1)}$	1,303,992 J
Arc-Flash Plasma Resistance	R_{AF}	0.00279 Ω
Arc-Flash Plasma Current	I_{AF}	17,917 A
Arc-Flash Plasma Power	P_{AF}	895,833 W
Arc-Flash Plasma Energy	E_{AF}	149,604 J

***Table II:** Arc-Flash (**AF**) parameters, symbols, & definitions; example of calculated or measured values; see figure 2*

Arc-Flash Initiation and Ignition Mechanisms; A Brief Note:

*Arc-faults have two main modes: an "in-series with the load mode" arc (**S-Arc**), and an "in-parallel with the power source mode" arc (**P-Arc**)[3]. An arc-flash is a **P-Arc** which may be initiated in two ways: (1) by electron field emission (**F-Arc-flash**), while undergoing a dielectric breakdown (aka, "flash-over"), or (2) by thermionic emission (**T-Arc-flash**), while experiencing an unintended metallic contact (aka, "arc-over"). The latter has typically been ignored in studies of arc-flash, however, must be considered when designing electronic arc-flash suppressors to fully address arc-flash events.*

Conclusion

One must appreciate the facts and myths, initiation and ignition mechanisms, and associated calculations of arc-flash (**AF**). For example, understanding the fact that most of the energy during an **AF** is dissipated inside the power source (in this case the transformer) dispels a significant **AF** myth. This and other myths have prevented the development of electronic arc-flash suppression (**EAFS**). The above bolted short circuit (**BSC**) and **AF** plasma ignition calculations provide further insights required to surmount arc-flash myths.

References:
1. IEEE Standards Association, "IEEE Guide for Performing Arc-Flash Hazard Calculations," IEEE Std 1584™-2018
2. R.Henke and R.P.Thorbus, "The Arc Species Zoo," 2021
3. R.Henke and R.P.Thorbus, "Parallel Arcs and Series Arcs," 2022

©2022 Arc Suppression Technologies. All rights reserved. All material presented is subject to change without notice. "NOsparc" is a registered trademark of Arc Suppression Technologies.